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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,649	11/24/2003	Kevin J. Lee	42P16018	4663

7590 05/13/2005

Jan Carol Little-Washington
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,649	LEE, KEVIN J.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *5-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

Applicants' amendment filed on February 22, 205 has been entered and forwarded to the Examiner on March 09, 2005.

Therefore claims 1-4 as recited in the amendment are currently pending in the Application.

Claims 5-29 are withdrawn as being drawn to a non-elected group and must be can celled (see below).

Election/Restrictions

This application contains claims 5-29 drawn to an invention nonelected with out traverse in Paper received on February 22, 2005 .

A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC # 1 03

The following is p quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action.

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior ad are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Meyer et al. (U.S. Patent No. 5,089,880, herein after Meyer) in view of Distefano et al. (U.S. Patent No. 5,558,ù28, herein after Distefano). (The previous rejection is reproduced below for response to Applicants' arguments see section below).

With respect to claim 1 Meyer describes an apparatus, comprising a first wafer having a first metal pattern disposed on a top surface; (Meyer, fig. 1 wafer 24 having metal pattern 36, col. 6 lines 1-2) a second wafer having a second metal pattern disposed on a top surface; (Meyer fig. 2 , wafer 22 having second metal pattern 36, col. 5 lines 67-68) and an interposer disposed between the top surface of the first wafer and the top surface of the second wafer, (Meyer figs. 4 to 6, # 26,62, col.6 lines 4-6,10-13, col. 8 lines 33-35) the interposer having a pattern of metal vias disposed (in. thermoplastic) (Meyer col. 6 line 7).

Meyer does not specifically describe its thermosetting plastic as being cured .

However Distefano, a patent from the same filed of endeavor, describes in col.I lines 65-67 and col.2 lines 1 to 9 describes cured thermosetting plastic to form an unitary mass and cause the flowable dielectric material to flow and conform to the major surface of the circuit panels the pattern of metal vias being aligned with and electrically coupled to the first metal pattern and the second metal pattern and to cross link the material of the thermosetting plastic .

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Distefano's cured thermosetting plastic instead of Meyer's un specified thermosetting plastic . The motivation to undedake the above combination is to form an unitary mass and cause the flowable dielectric material to flow and conform

to the major surface of the circuit panels the pattern of metal vias being aligned with and electrically coupled to the first metal pattern and the second metal pattern .(Distefano col. 2 lines 4-5 and col. Col. 4 line 65 to col. 5 line 9) and to cross link the material of the thermosetting plastic .

With respect to claim 2 Meyer describes the apparatus of claim 1, wherein the interposer further comprises of the dielectric film disposed in the cured thermosetting plastic. (Meyer col.8 lines 45-48).

With respect to claim 3 Meyer describes the apparatus of claim I , wherein the cured thermosetting plastic comprises a polyimide material. (Meyer col. 8 line 46).

With respect to claim 4 Meyer describes the apparatus of claim 3, wherein the cured thermosetting plastic comprises an epoxy material.(Distefano col. 8 lines 49-51).

Response to Arguments

Applicant's arguments filed on 02/22/2005 have been fully considered but they are not persuasive. for the following reasons:

Applicants' first contention that Myer " does not appear to be directed to stacking multiple circuit boards, but planes within a single printed circuit board" is based on lack of understanding and/or an incomplete analysis of Myers' description.

Myer for example describes for e.g. in its abstract last 9 lines :

cal isolation. The plurality of layers, or wafers, includes signal wafers and ground/voltage wafers. The signal wafers are formed of a low dielectric constant material to optimize the propagation velocity of signals traveling in signal traces connecting selected segments in the signal wafer. More than 100 wafers may be provided in a microstack and repairs and revisions of conductor routing are easily accomplished by substituting new wafers within the microstack.

Therefore Myer describes its micro stack as including plurality of layers or plurality of wafers , further Myer specifically teaches its microstack as including 100 wafers .(emphasis supplied).

Further Myer in col. 5 lines 34-35 cited by Applicants' in support of their position that does not appear to be directed to stacking multiple circuit boards, but planes within a single printed circuit board is at complete odds with Myers' teaching in the cited col.5 lines 34-35 (reproduced below).

A microstack 20 provides electrical interconnections between selected ones of the contacts 16 of semiconductor devices 14. The microstack 20 includes alternating signal wafers 22 and ground/voltage wafers 24. Each wafer 22, 24 has a plurality of segments 26 provided in an array so that aligned segments 26 in wafers 22, 24 form columns 28 (FIGS. 2 and 3). Each column 28 is

A microstack 20 provides electrical interconnections between selected ones of the contacts 16 of semiconductor devices 14. The microstack 20 includes alternating signal wafers 22 and ground/voltage wafers 24. Each wafer 22, 24 has a plurality of segments 26 provided in an array so that aligned segments 26 in wafers 22, 24 form columns 28 (FIGS. 2 and 3). Each column 28 is

Therefore it is not understood how Applicants' can conclude that Myer " does not appear to be directed to stacking multiple circuit boards, but planes within a single printed circuit board" . Therefore Applicants' arguments are persuasive.

Applicants' second contention that "DeStefano also appears to be directed to stacking of individual layers to fabricate a printed circuit board" is also not persuasive for the following reasons :

a) As shown above the primary reference teaches/suggests including plurality of layers or plurality of wafers , further Myer specifically teaches its microstack as including 100 wafers .(emphasis supplied). Therefore it is not necessary for the secondary reference to repeat the teachings /suggestions of the primary reference .

If both references individually taught all the limitations the previous rejection would have been a 102 anticipatory rejection and not a 103 rejection based on the combined teachings of Myer and Destefano.

b) Applicants' are arguing what each applied reference does not teach whereas the rejection is based on the combined teachings of the applied references.

The above describes piece meal analysis cannot negate obviousness, as stated in In re Keller , 208 USPQ 871 (CCPA 1981), " In response to Applicants' piece meal analysis of the references, it has been held that cannot show non-obviousness by attacking references individually where as, here , the rejections are based on combinations of references ."

c) Destefano contrary to Applicants' contention at least in figure 2 (elements 10 a and 10 b and col. 4 lines 57 to 65 (reproduced below) describes multiple circuit panels which circuit panels are defined in col. 1 lines 15-16 as " electrical components are commonly mounted on circuit panel structures such as circuit boards. " (emphasis supplied) .

interconnect locations may be flowable. A method according to this aspect of the invention preferably includes the step of stacking the circuit panels and interposers in superposed relation so that each interposer is disposed between two circuit panels, with the major surfaces of the interposers and circuit panels confronting one another, and with interconnect locations on the confronting surfaces of the circuit panels and interposers being aligned with one another. The method most preferably further includes the step of causing the flowable dielectric material to flow and conform to the major surfaces of the circuit panels. The method desirably includes

interconnect locations may be flowable. A method according to this aspect of the invention preferably includes the step of stacking the circuit panels and interposers in superposed relation so that each interposer is disposed between two circuit panels, with the major surfaces of the interposers and circuit panels confronting one another, and with interconnect locations on the confronting surfaces of the circuit panels and interposers being aligned with one another. The method most preferably further includes the step of causing the flowable dielectric material to flow and conform to the major surfaces of the circuit panels. The method desirably includes

Therefore DeStefano contrary to Applicants' contentions teaches stacking of individual circuit boards (i.e. circuit panels) and not individual layers to fabricate a printed circuit board.

Therefore all of Applicants' contentions are not persuasive and the all claims are finally rejected.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571) 272 - 1718. The examiner can normally be reached on 8.00 to 5.00.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven H. Rao
Patent Examiner
May 03, 2005.

LONG PHAM
PRIMARY EXAMINER